

IN THE CLAIMSListing of Claims:

- 1        1.        (original) A receiver circuit for terminating a transmission line comprising:  
2                a receiver having an input coupled to a transmission line output of said  
3        transmission line forming a common node, an output generating a digital signal in  
4        response to a signal at said transmission line output and a threshold voltage;  
5                a termination network coupled to said common node for setting a plurality of  
6        Thevenins voltages and Thevenins impedances in response to a plurality of control  
7        signals; and  
8                logic circuitry for generating said plurality of control signals in response to a  
9        plurality of mode setting inputs.
- 1        2.        (previously presented) A receiver circuit for terminating a transmission line  
2        comprising:  
3                a receiver having an input coupled to a transmission line output of said  
4        transmission line forming a common node, an output generating a digital signal in  
5        response to a signal at said transmission line output and a threshold voltage;  
6                a termination network coupled to said common node for setting a plurality of  
7        Thevenins voltages and Thevenins impedances in response to a plurality of control  
8        signals; and  
9                logic circuitry for generating said plurality of control signals in response to a  
10       plurality of mode setting inputs, wherein said termination network comprises a first  
11       termination network coupled to said common node and setting a Thevenins impedance  
12       and a Thevenins voltage at said common node and a second termination network coupled  
13       to said common node and modifying said Thevenins impedance and said Thevenins  
14       voltage in response to first and second control signals.
- 1        3.        (original) The circuit of claim 2 further comprising a third termination network  
2        coupled to said common node and modifying said Thevenins impedance and said

3 Thevenins voltage in response to third and fourth control signals generated by said logic  
4 circuitry.

1 4. (original) The circuit of claim 2, wherein said first termination network is  
2 coupled to said common node in response to fifth and sixth control signals generated by  
3 said logic circuitry.

1 5. (currently amended) The circuit of claim 4, wherein said second ~~first~~ termination  
2 network comprises:

3 a first resistor having a first terminal coupled to a first power supply voltage with  
4 a first electronic switch in response to a first logic state of said first control signal and a  
5 second terminal;

6 a second resistor having a first terminal coupled to said second terminal of said  
7 first resistor and said common node and a second terminal coupled to a second power  
8 supply voltage with a second electronic switch in response to a first logic state of said  
9 second control signal.

1 6. (currently amended) The circuit of claim ~~[[2]]~~3, wherein said third ~~second~~  
2 termination network comprises:

3 a first resistor having a first terminal coupled to said first power supply voltage  
4 with a first electronic switch in response to a first logic state of said third control signal  
5 and a second terminal;

6 a second resistor having a first terminal coupled to said second terminal of said  
7 first resistor and said common node and a second terminal coupled to a second power  
8 supply voltage with a second electronic switch in response to a first logic state of said  
9 fourth control signal.

1       7.       (currently amended) The circuit of claim ~~[[3]]~~4, wherein said first ~~third~~  
2       termination network comprises:

3               a first resistor having a first terminal coupled to said first power supply voltage  
4       with a first electronic switch in response to a first logic state of said fifth control signal  
5       and a second terminal;

6               a second resistor having a first terminal coupled to said second terminal of said  
7       first resistor and said common node and a second terminal coupled to said second power  
8       supply voltage with a second electronic switch in response to a first logic state of said  
9       sixth control signal.

1       8.       (original) The circuit of claim 2, wherein said receiver circuit is a logic gate  
2       having a first logic input coupled to said receiver input, a second logic input coupled to a  
3       voltage corresponding to a first logic state, wherein said threshold voltage is a switching  
4       voltage of said logic gate and is generated internal to said logic gate.

1       9.       (original) The circuit of claim 2, wherein said receiver circuit is a comparator  
2       having a positive input coupled to said input of said receiver, a negative input coupled to  
3       said threshold voltage and a comparator output coupled to said receiver output.

1       10.      (original) The circuit of claim 4, wherein said receiver circuit is a comparator  
2       having a positive input coupled to said input of said receiver, a negative input coupled to  
3       said threshold voltage and a comparator output coupled to said receiver output.

1       11.      (original) The circuit of claim 7, wherein said threshold voltage is equal to one  
2       half the difference between said first and second power supply voltages.

1       12.      (currently amended) The circuit of claim 4, wherein said mode inputs comprise a  
2       first mode input for setting said Thevenins impedance to substantially match a  
3       characteristic impedance of said ~~TL~~ transmission line (TL) and said Thevenins voltage to

4 substantially match said threshold voltage, wherein said first, second, ~~fourth and fifth~~ and  
5 sixth electronic switches are gated ON by said first, second, ~~fourth and fifth~~ and sixth  
6 control signals.

1 13. (original) The circuit of claim 12, wherein said mode inputs comprise a second  
2 mode for setting said Thevenins impedance to substantially match a characteristic  
3 impedance of said TL and said Thevenins voltage to greater than said threshold voltage,  
4 wherein said first, second, third and fifth electronic switches are gated ON by said first,  
5 second, third and fifth control signals.

1 14. (original) The circuit of claim 13, wherein said mode inputs comprise a third  
2 mode for setting said Thevenins impedance to substantially match a characteristic  
3 impedance of said TL and said Thevenins voltage to less than said threshold voltage,  
4 wherein said first, second fourth and sixth electronic switches are gated ON by said first,  
5 second fourth and sixth control signals.

1 15. (original) The circuit of claim 14, wherein said mode inputs comprise a fourth  
2 mode for setting said Thevenins impedance to greater than a characteristic impedance of  
3 said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein  
4 said first and second electronic switches are gated on by said first and second control  
5 signals.

1 16. (original) The circuit of claim 15, wherein said mode inputs comprise a fifth  
2 mode for setting said Thevenins impedance to less than a characteristic impedance of  
3 said TL and said Thevenins voltage to substantially equal said threshold voltage, wherein  
4 said first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said  
5 first, second, third, fourth, fifth, and sixth control signals.

1 17. (original) The circuit of claim 16, wherein said mode inputs comprise a driver  
2 mode wherein said first, second, and third termination networks operate as a driver

3 circuit for impressing a drive signal on said common node in response to logic states of a  
4 driver signal controlling said first, second, third, fourth, fifth and sixth control signals,  
5 wherein said second, fourth and sixth electronic switches are gated ON by a first logic  
6 state of said driver signal and said first, third, and fifth electronic switches are gated ON  
7 by a second logic state of said driver signal.

1 18. (original) The circuit of claim 15, wherein said logic circuitry comprises:  
2 circuitry for alternating between selected of said first, second, third, fourth, and  
3 fifth modes in response to a first logic state of a dynamic enable signal and logic states of  
4 a modified receiver output signal;  
5 a state circuit for generating said modified receiver signal in response to said  
6 receiver output signal and a selected delay time .

1 19. (original) The circuit of claim 18, wherein said modified receiver transitions to a  
2 first logic state said delay time after said receiver output signal transitions to said first  
3 logic state and to a second logic state said selected delay time after said receiver signal  
4 transitions to said second logic state, wherein said selected delay time is set by delay  
5 control signal.

1 20. (original) The circuit of claim 19, wherein said circuitry switches to said fourth  
2 mode when said modified receiver signal has a first logic state and switches to said fifth  
3 mode when said modified receiver signal has a second logic state.

1 21. (original) The circuit of claim 18, wherein said first logic state of said dynamic  
2 mode signal is set in response to a selected signal quality parameter of said receiver  
3 output signal.

1       22.     (original) An integrated circuit (IC) comprising:  
2             a digital processor;  
3             memory for storing instructions and data for said processor;  
4             input/output (I/O) interface circuitry for communicating to device circuitry  
5     external to said IC;  
6             a receiver circuit in said interface circuitry for terminating a transmission line  
7     coupling said receiver circuit to said device circuitry, said receiver circuit further  
8     comprising;  
9             a receiver having an input coupled to a transmission line output of said  
10    transmission line forming a common node, an output generating a digital signal in  
11    response to a signal at said transmission line output and a threshold voltage;  
12             a termination network coupled to said common node for setting a plurality of  
13    Thevenins voltages and Thevenins impedances in response to a plurality of control  
14    signals; and  
15             logic circuitry for generating said plurality of control signals in response to a  
16    plurality of mode setting inputs.

1       23.     (previously presented) An integrated circuit (IC) comprising:  
2             a digital processor;  
3             memory for storing instructions and data for said processor;  
4             input/output (I/O) interface circuitry for communicating to device circuitry  
5     external to said IC;  
6             a receiver circuit in said interface circuitry for terminating a transmission line  
7     coupling said receiver circuit to said device circuitry, said receiver circuit further  
8     comprising;  
9             a receiver having an input coupled to a transmission line output of said  
10    transmission line forming a common node, an output generating a digital signal in  
11    response to a signal at said transmission line output and a threshold voltage;

12 a termination network coupled to said common node for setting a plurality of  
13 Thevenins voltages and Thevenins impedances in response to a plurality of control  
14 signals; and

15 logic circuitry for generating said plurality of control signals in response to a  
16 plurality of mode setting inputs, wherein said termination network comprises a first  
17 termination network coupled to said common node for setting a Thevenins impedance  
18 and a Thevenins voltage at said common node and a second termination network coupled  
19 to said common node for modifying said Thevenins impedance and said Thevenins  
20 voltage in response to first and second control signals.

1 24. (original) The IC of claim 23 further comprising a third termination network  
2 coupled to said common node and modifying said Thevenins impedance and said  
3 Thevenins voltage in response to third and fourth control signals generated by said logic  
4 circuitry.

1 25. (original) The IC of claim 23, wherein said first termination network is coupled  
2 to said common node in response to fifth and sixth control signals generated by said logic  
3 circuitry.

1 26. (currently amended) The IC of claim 25, wherein said second ~~first~~ termination  
2 network comprises:

3 a first resistor having a first terminal coupled to a first power supply voltage with  
4 a first electronic switch in response to a first logic state of said first control signal and a  
5 second terminal;

6 a second resistor having a first terminal coupled to said second terminal of said  
7 first resistor and said common node and a second terminal coupled to a second power  
8 supply voltage with a second electronic switch in response to a first logic state of said  
9 second control signal.

1 27. (currently amended) The IC of claim ~~[[23]]~~24, wherein said third ~~second~~  
2 termination network comprises:

3 a first resistor having a first terminal coupled to said first power supply voltage  
4 with a first electronic switch in response to a first logic state of said third control signal  
5 and a second terminal;

6 a second resistor having a first terminal coupled to said second terminal of said  
7 first resistor and said common node and a second terminal coupled to a second power  
8 supply voltage with a second electronic switch in response to a first logic state of said  
9 fourth control signal.

1 28. (currently amended) The IC of claim ~~[[24]]~~25, wherein said first ~~third~~  
2 termination network comprises:

3 a first resistor having a first terminal coupled to said first power supply voltage  
4 with a first electronic switch in response to a first logic state of said fifth control signal  
5 and a second terminal;

6 a second resistor having a first terminal coupled to said second terminal of said  
7 first resistor and said common node and a second terminal coupled to said second power  
8 supply voltage with a second electronic switch in response to a first logic state of said  
9 sixth control signal.

1 29. (original) The IC of claim 23, wherein said receiver circuit is a logic gate having  
2 a first logic input coupled to said receiver input, a second logic input coupled to a voltage  
3 corresponding to a first logic state, wherein said threshold voltage is a switching voltage  
4 of said logic gate and is generated internal to said logic gate.

1 30. (original) The IC of claim 23, wherein said receiver circuit is a comparator  
2 having a positive input coupled to said input of said receiver, a negative input coupled to  
3 said threshold voltage and a comparator output coupled to said receiver output.



1 31. (original) The IC of claim 25, wherein said receiver circuit is a comparator  
2 having a positive input coupled to said input of said receiver, a negative input coupled to  
3 said threshold voltage and a comparator output coupled to said receiver output.

1 32. (original) The IC of claim 28, wherein said threshold voltage is equal to one half  
2 the difference between said first and second power supply voltages.

1 33. (currently amended) The IC of claim 25, wherein said mode inputs comprise a  
2 first mode input for setting said Thevenins impedance to substantially match a  
3 characteristic impedance of said ~~TL~~ transmission line (TL) and said Thevenins voltage to  
4 substantially match said threshold voltage, wherein said first, second, fourth and fifth  
5 electronic switches are gated ON by said first, second, fourth and fifth control signals.

1 34. (original) The IC of claim 33, wherein said mode inputs comprise a second mode  
2 for setting said Thevenins impedance to substantially match a characteristic impedance of  
3 said TL and said Thevenins voltage to greater than said threshold voltage, wherein said  
4 first, second, third and fifth electronic switches are gated ON by said first, second, third  
5 and fifth control signals.

1 35. (original) The IC of claim 34, wherein said mode inputs comprise a third mode  
2 for setting said Thevenins impedance to substantially match a characteristic impedance of  
3 said TL and said Thevenins voltage to less than said threshold voltage, wherein said first,  
4 second fourth and sixth electronic switches are gated ON by said first, second fourth and  
5 sixth control signals.

1 36. (original) The IC of claim 35, wherein said mode inputs comprise a fourth mode  
2 for setting said Thevenins impedance to greater than a characteristic impedance of said  
3 TL and said Thevenins voltage to substantially equal said threshold voltage, wherein said  
4 first and second electronic switches are gated on by said first and second control signals.

1       37.     (original) The IC of claim 36, wherein said mode inputs comprise a fifth mode  
2       for setting said Thevenins impedance to less than a characteristic impedance of said TL  
3       and said Thevenins voltage to substantially equal said threshold voltage, wherein said  
4       first, second, third, fourth, fifth, and sixth electronic switches are gated ON by said first,  
5       second, third, fourth, fifth, and sixth control signals.

1       38.     (original) The IC of claim 37, wherein said mode inputs comprise a driver mode  
2       wherein said first, second, and third termination networks operate as a driver circuit for  
3       impressing a drive signal on said common node in response to logic states of a driver  
4       signal controlling said first, second, third, fourth, fifth and sixth control signals, wherein  
5       said second, fourth and sixth electronic switches are gated ON by a first logic state of  
6       said driver signal and said first, third, and fifth electronic switches are gated ON by a  
7       second logic state of said driver signal.

1       39.     (original) The IC of claim 36, wherein said logic circuitry comprises:  
2       circuitry for alternating between selected of said first, second, third, fourth, and  
3       fifth modes in response to a first logic state of a dynamic enable signal and logic states of  
4       a modified receiver output signal;  
5       a state circuit for generating said modified receiver signal in response to said  
6       receiver output signal and a selected delay time .

1       40.     (original) The IC of claim 39, wherein said modified receiver transitions to a first  
2       logic state said delay time after said receiver output signal transitions to said first logic  
3       state and to a second logic state said selected delay time after said receiver signal  
4       transitions to said second logic state, wherein said selected delay time is set by delay  
5       control signal.

1       41.     (original) The IC of claim 40, wherein said circuitry switches to said fourth mode  
2       when said modified receiver signal has a first logic state and switches to said fifth mode  
3       when said modified receiver signal has a second logic state.

1       42.     (original) The IC of claim 39, wherein said first logic state of said dynamic mode  
2       signal is set in response to a selected signal quality parameter of said receiver output  
3       signal.